IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING APPLICATION UNDER RULE 53(b)

Pursuant to 37 CFR 1.53(b), please file a ☒ continuation/☐ divisional of the pending prior PATENT APPLICATION OF:
Inventor: STEWART et al.
Serial No. 09/294,591
Filed: April 20, 1999
For: **TWISTED PAIR COMMUNICATIONS LINE SYSTEM**

JC863 U.S. PTO
06/30/00

Atty Dkt.: 2540-248
C# M#
Date: June 30, 2000
Group: 2734
Examiner: Y. Tse

JC863 U.S. PTO
09/608142
06/30/00

Assistant Commissioner for Patents
Washington, DC 20231
Sir:

This request for filing under Rule 53(b) is made by the following named inventor(s) (using the above-identified title):
Inventor(s): STEWART et al.

☐ Attached is a copy of a declaration from a prior application (37 C.F.R. § 1.63(d).
☐ Priority is hereby claimed under 35 USC 119 based on the following foreign applications, the entire content of which is hereby incorporated by reference in this application:

Application Number	Country	Day/Month/Year/Filed

☐ certified copy(ies) of foreign application(s) attached or
☐ already filed on _____ in prior appln. no. _____ filed _____
☐ already filed in _____ filed _____

☐ Please amend the specification by inserting before the first line: -- This application claims the benefit of U.S. Provisional Application No. , filed , the entire content of which is hereby incorporated by reference in this application.--
☒ The prior application is assigned to Cybex Computer Products Corporation.
☒ Power of Attorney has been granted to J. Scott Davidson et al, Reg. No. 33,489 of Nixon & Vanderhye P.C., 1100 N. Glebe Rd., 8th Floor, Arlington, VA 22201.
☒ Address all future communications to: Nixon & Vanderhye P.C., 1100 N. Glebe Rd., 8th Floor, Arlington, VA 22201.
☐ Please amend the specification by inserting before the first line --This is a of application Serial No. , filed , now pending, the entire content of which is hereby incorporated by reference in this application.--
☐ "Small entity" statement of record. ☐ "Small entity" statement attached.
☐ Petition filed in prior application to extend its life to insure copendency.
☒ The Examiner's attention is directed to the prior art cited in the parent application by applicant and/or Examiner for the reasons stated therein.
☐ Please enter the attached and/or below preliminary amendment **prior** to calculation of filing fee:

☒ The entire disclosure of the prior application above-referenced is considered as being part of the disclosure of this new application and is hereby incorporated by reference therein.

FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY HEREWITH CANCELED

Basic Filing Fee					$	690.00
Total effective claims	52	- 20 (at least 20) =	32	x $ 18.00	$	576.00
Independent claims	9	- 3 (at least 3) =	6	x $ 78.00	$	468.00
If any proper multiple dependent claims now added for first time, add $260.00 (ignore improper)					$	0.00
				SUBTOTAL	$	1734.00
If "small entity," then enter half (1/2) of subtotal and subtract					-$(	0.00)
				SECOND SUBTOTAL	$	1734.00
Assignment Recording Fee ($40.00)					$	40.00
				TOTAL FEE ENCLOSED	$	1774.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

Attachments: Inventors Declaration

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Our Ref.: **2540-248**

U.S. PATENT APPLICATION

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Invention: TWISTED PAIR COMMUNICATIONS LINE SYSTEM

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SPECIFICATION

TWISTED PAIR COMMUNICATIONS LINE SYSTEM

Cross Reference of Related Applications

This application is a continuation of Application Serial No. 09/294,591, filed April 20, 1999 (which is incorporated herein by reference), which is a continuation of Application Serial No. 08/744,629, filed November 6, 1996, now U.S. Patent No. 5,926,509, issued July 20, 1999 (which is incorporated herein by reference), which is a continuation-in-part of Application Serial No. 08/660,076, filed June 3, 1996, which in turn is a continuation-in-part of Application Serial No. 08/177,442, filed January 5, 1994, now abandoned. The said Application Serial No. 08/744,629 also claims the benefit of Provisional Application Serial No. 60/010,741, filed January 29, 1996, and is a continuation-in-part of Application Serial No. 08/741,697, filed October 31, 1996, which is a continuation-in-part of Application Serial No. 08/219,979, filed March 29, 1994, now U.S. Patent No. 5,576,723, issued November 19, 1996.

1. Field of the Invention

The invention relates generally to the transmission of wideband signals over relatively cheap, low-grade cable.

BACKGROUND AND SUMMARY OF THE INVENTION

It is now commonplace to locate computers, keyboards, and monitors, particularly color monitors, at spaced locations in a building or buildings. These locations often are several hundred feet apart, requiring that where analog color signals are involved that there must be transmitted three separate color signals, each having an approximate frequency range from D.C. up to 200 MHZ. Thus, there is a requirement that appropriate transmission lines be in place, or be installed, to accommodate such transmissions. As is well known, either fiber optic or multiple coaxial cables may normally be employed, but such is often not available. Thus, there may be required by an occupant of a building that appropriate signal conductors be after fitted to the building. This can result in a considerable cost. Ideally, there would be present, or there might be installed at a relatively low cost, lower-grade conductors, such as network cable or twisted pair cable and that it be somehow used.

In a co-pending application, application Serial No 08/177,442, the existing cable was of the digital network type, for example, having 15 conductors within an outer shield and designed to carry on the order of 2,400 baud rate signals and wherein there existed straight (untwisted) conductors.

The problem in that case was to overcome frequency deficiencies and to overcome interaction between colors as finally received. The solution was that of discovering appropriate

frequency-amplitude compensation plus effecting a phase reversal of one color signal appearing on one conductor (with respect to shield) and positioning this conductor between conductors carrying the other two color signals. At the receiver, the phase reversal was reversed back.

The present invention deals with a second type of cable, basically telephone (voice frequency) cable wherein there is included a plurality of twisted pair-type conductors, typically four pairs for the carrying of as many communications.

It too has unique problems with respect to frequency compensation. A second problem appears from the finding that different sets of twisted pairs, and in different cables, have a variety of twist rates, different twist rates for a given cable being provided to prevent telephone cross-talk between communications on different twisted pairs of a cable. Unfortunately, the applicants have found that the latter was a culprit in preventing good color signal transmissions since a composite of three color signals, sent on separate twisted pairs, is required, and the different twist rates of conductor pairs caused the lengths of the pairs and signal delays to differ. This in turn resulted in the receipt of a composite of color signals with observable impurities and thus an unsatisfactory presentation on a color monitor.

Significant, however, was the substantial availability of such cable and that it is already installed in many buildings where color transmissions were now needed. Thus, if it could be employed, such would enable a tremendous saving, a mark of clear

technical achievement in view of the fact that the problem has remained unsolved for at least 10 years.

The applicants have discovered that relatively high frequency color video signals may be transmitted with high color purity over a cable having multiple, relatively low frequency, twisted pair telephone lines and despite their having different twist rates, which rates are non-uniform as between cable manufacturers. The applicants have solved the problem by effecting certain selected frequency compensation to color signals at each end of a cable and by discretely applying delays to the two twisted pair lines having lower twist rates. Alternately, in certain instances, applicants have discovered that adequate color purity can be achievable over cable runs of 300 feet or less by connecting the red video signals to the twisted pairs having the smallest twist rate (i.e., lowest twist rate), the green video signals to the twisted pair having the next highest twist rate, and the blue video signals through the twisted pair having the third largest twist rate. Typically, then, the synchronization signals would be connected through the cable having the largest twist rate (or tightest twist rate), which is not as critical.

BRIEF DESCRIPTION OF THE DRAWINGS

These, as well as other objects and advantages of this invention, will be more completely understood and appreciated by careful study of the following more detailed description of a

presently preferred exemplary embodiment of the invention taken in conjunction with the accompanying drawings, of which:

Figure 1 is a combination schematic/block diagram of an input amplifier configuration;

Figure 1a is a combination block/schematic illustration of the transmitter portion of applicants' system;

Figure 1b is a combination block/schematic diagram of the receiver portion of applicants' system;

Figure 2 is a schematic illustration of a portion of the circuitry shown in block form in Figure 1a;

Figure 3 is a pictorial view, partially broken away, of a delay line assembly employable in applicants' system;

Figure 4 is a sectional view as seen along line 4-4 of Figure 3;

Figure 5 is a schematic illustration of a delay line partially shown in Figures 3 and 4 and particularly illustrating that selected portions may be employed for selected delays; and

Figure 6 is a schematic illustration of a portion of Figure 1b shown in block form.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Referring initially to Figure 1, a non-inverting, constant current amplifier 101 is shown having an input region 103 and an

output region 107. Input region 103 is particularly coupled to source 108 of degraded analog video signals, such as found in the assignee's Commander™ module, with resultant lowered amplitude and attenuation of high frequency components of the signal as shown in Figure 1 as being derived from a computer switched by switching circuit 108a from a particular computer of computers 108b. In this embodiment wherein the Commander™ module is used, an output analog video signal is provided by an emitter 126 of a PNP transistor 117 in the Commander™ module. Output region 107 of amplifier 101 is coupled to a load having known characteristics, such as an analog video monitor 118 or other analog device, with amplifier 101 providing a non-inverted, amplified representation of the input signal across the load. Where the output is coupled to a conventional analog VGA computer monitor 118, the monitor represents a load 119, which may be a resistor of about 75 ohms, with the output signal from region 107 across this 75 ohm load being about 700 millivolts. In this instance, it is to be appreciated that there would be a discrete circuitry 101 for each of the discrete video signals which, in the instance of a VGA monitor, include primary red, green, and blue analog signals. While this circuitry in a preferred embodiment is to be implemented with respect to the currently manufactured Commander™ module, it will be apparent to those skilled in the art that numerous other applications exist where non-inverting analog amplification with an enhanced output is required or desired.

Network 131, an impedance including a capacitive reactance, as will be described, is coupled from the input emitter 126 of transistor 117 to the emitter of transistor 123. Generally, in the Commander™ module, PNP transistor 117 is coupled in emitter-follower configuration and connected to network 131, with a base 120 of transistor 117 being coupled to a relatively weak analog video input signal. As such, collector 121 of transistor 117 is coupled to ground, providing an alternate current path to ground for the video signal. Resistor 128 of network 131 has a value of about 20 ohms, and capacitor 129 has a value of about 220 pF, network 131 serving to divert current in a direct relationship from the load impedance responsive to positive voltage excursions of the input signal applied to base 120. Impedance network 131 may be fixed to provide a generally fixed gain amplifier or one which can provide variable gains and in selected frequency ranges, the impedance including capacitive reactance and this reactance is coupled as shown between emitter 126 and emitter 125 of transistors 117 and 123. It is chosen to approximately equal the combined reactance effects of transistors 127 and 123 and a cable connected to a load 119. Collector 134 of transistor 123, as an example, is coupled across a load impedance 119 to the input of a conductor of a communications cable. As an example, for transistors 117 and 123, one may employ a transistor 2N2907a or equivalent, which is characterized by having a typical current gain of about 200 and is further able to maintain constant emitter voltage for a given base voltage. Typically, several reactance sets

of RC may be employed, the choice being as to number and value for particular frequency ranges to be high frequency boosted, which in turn is a function of transistor effects of transistors 117 and 123 and the length of a cable.

A constant current source 136, which may be a conventional one, such as a fixed bias transistor, coupled to a stable voltage source, e.g., 4.5 volts, is coupled to terminal 140 between network 131 and emitter 119 and provides a current limited source of about 9.33 milliamps to be divided between network 131 and transistor 123. A voltage divider circuit 142 includes a resistor 144 coupled at one end to the 4.5-volt voltage source at terminal 138 and at an opposite end to terminal 152, also coupled to base 148 of transistor 123. A second resistor 150 is coupled at one end to a ground potential and at an opposite end to junction 152, with values of resistors 144 and 150 selected to provide a potential to base 148 of transistor 123 no lower than a highest anticipated peak input potential of the analog signal at the base of transistor 117, including any D.C., offset that may be present.

In the Commander™ module, it has been found that the analog video signal may be degraded to about 450 millivolts with a positive 150-millivolt D.C. offset. Thus, values of resistors 144 and 150 are selected to provide about 650 millivolts to terminal 152. With the described voltages applied to transistor 123, a lowest input signal at the input diverts current flow from transistor 123 to flow through resistor 128, reducing current flow through transistor 123 and the voltage at terminal 138 to a point where

transistor 123 is biased in its operating range just above its cutoff point. As the input signal increases, current flow through resistor 128 decreases, slightly increasing a voltage level at terminal 140, biasing transistor 123 to a more conductive state and resulting in more current flow through transistor 123 and in turn increasing potential 107, for example, monitor 118, in direct relation with the input signal.

In the instance where the signal from source 108 is of lowered amplitude and is attenuated, but possesses sufficient current sourcing capabilities to drive network 131, the analog input signal is the input signal coupled directly to network 131, as represented by dashed line 154. In this configuration, resistors 144 and 150 are selected to provide a voltage at terminal 152 of about 650 millivolts below a highest anticipated peak input potential of the analog signal in order to compensate for elimination of the diode drop of transistor 117. Additionally, an output driver of routing circuit 108 would also be conventionally configured to provide an alternate current path to ground, as illustrated by ground 126. In this instance, when the input signal is at a lower state, current flows from current source 36 through network 131 to ground 127.

While the specific example described above which includes transistor 117 is an application tailored for the Commander™ module wherein the load is resistive in nature, a more generalized representation of the instant invention without transistor 117 may be illustrated where both load and bypass impedances are complex

impedances. Theoretically, and assuming a transistor has a high current gain for transistor 123, the impedance of network 131 may be represented as Z_b, with the analog signal source voltage represented by V_i, which in this instance, is coupled directly to load 119 (dashed line 154), and the highest excursion of the analog signal defined by V_x. Current through impedance Z_b, is represented as I_1. The voltage applied to base 148 is represented as $V_f = V_x$ peak - 0.650, and, as stated, is selected to be no lower than the highest peak amplitude of the input signal V_x minus the approximately 650-millivolt diode drop of the emitter-base junction of transistor 123. With such voltages applied to transistor 123, the voltage at junction 140 only fluctuates slightly due to the fixed base voltage and the forward biased emitter-base junction of transistor 123, with this slight fluctuation being sufficient to directly vary conductivity of transistor 123 and resultant current flow therethrough with respect to the input signal. This generally constant voltage at junction 140 is represented by V_x (max peak amplitude), with I_c being current from constant current supply 136. The load is represented by Z_L, a complex impedance, with current flow through the load represented as I_2 and voltage across load Z_L represented as V_o. With such designations, voltage across the load is defined by:

$$V_o = I_2 \times Z_L$$

and the constant current into junction 140 is a sum of the output currents, or:

$$I_C = I_1 + I_2$$

The deflected current through impedance Z_b is defined by:

$$I_C = V_X - V_1 / Z_b$$

with the inversely proportional flow of current through load Z_L defined by :

$$I_2 \text{ x } - I_C - I_i = I_C - V_X - V_1 / Z_b$$

and the voltage across the load defined by:

$$V_o = Z_L I_2 = (I_2 V_X - V / Z_b) \text{ x } Z_L$$

For a change of input voltage V_i,

$$VP_o = (I_C - V_X - V_1 / Z_b) \text{ x } Z_L = (0 - (0 - V_1) / Z_b) \text{ x } Z_L$$

which, when resolved, becomes:

$$V_o = V_i / Z_b \text{ x } Z_i$$

yielding an A.C. gain of:

$$V_o / V_i = Z_L / Z_b$$

Thus, it is seen that gain of the amplifier is strictly controlled by load impedance and impedance between the emitters. In the specific example given for the Commander™ module, impedance of load Z_b, is about 75 ohms resistive, the magnitude of impedance of network 131 at a D.C. potential is about 20 ohms, and at 30 MHZ, is about 0.6 ohms, as given by the generalized circuit analysis in the foregoing and familiar to anyone skilled in the art. Therefore, it is demonstrated that the above-described amplifier of the preferred embodiment possesses frequency sensitive gain which varies from a gain of about 75/20 -

3.75 (Z_L divided by Z_b,) at a D.C. level and a gain of about 75/0.6 = 125 at 30 MHZ. For the various embodiments illustrated and described hereinafter, the coupling impedance is first determined and gain calculated by dividing load impedance by the coupling impedance.

In operation, and referring to Figure 1, a degraded analog video signal voltage referenced to ground from the Commander™ module taken from one of a plurality of computers C (only one shown) and intended to be applied to an analog computer monitor is applied to base 120 of transistor 117. In this instance, bias voltages of transistors 117 and 123 are obtained from terminal 140, with a reference voltage of about 600 millivolts taken from terminal 138 and applied to base 148 of transistor 123. The voltage at terminal 140 is about 1.2 volts, which is a diode drop of about 650 millivolts above the reference voltage applied to base 148, and which is varied as described by transistor 117 responsive to excursions of the input signal applied to base 120. The input signal is degraded to the extent of loss of high frequencies necessary and is offset by a positive D.C. bias of about 150 millivolts due to switching levels in the Commander™ module and degraded in amplitude to have a swing of about 450 millivolts between about 150 millivolts and 600 millivolts. This signal, when at the 150-millivolt level and applied to base 120 of transistor 117, biases transistor 117 on, deflecting virtually all the 9.33 milliamps from current source 136 through 20 ohm resistor 128 due to the difference of voltage potentials on either side of

resistor 128, with this current being applied to ground via transistor 117. This depletes current flow through transistor 123 and reduces voltage at terminal 140 to just above a cutoff voltage, reducing the IR voltage drop across the monitor load to 0 volts. As the input signal applied to base 120 rises to about 600 millivolts, transistor 117 is biased toward its cutoff region; and with about 1.2 volts applied to emitter 126 from terminal 140, less current flows through network 131 due to decreasing potential difference across resistor 128. This in turn slightly increases potential at terminal 140 such that transistor 123 is biased more toward a conductive state, resulting in increasing current flow through transistor 123 to the 75 ohm load in monitor 118. As the potential across network 13 equilibrates as transistor 117 is driven toward cutoff, the entire 9.33 milliamps from constant current source 136 is shifted to flow through transistor 123 and the 75 ohm monitor load, increasing the potential across the 75 ohm load to about 700 millivolts, a conventional level for an analog monitor.

As described, as the input signal fluctuates between low and high levels, the constant current is divided and fluctuates with the input-signal between transistors 117 and 123. In the absence of transistor 117, an analog video signal extending from about 150 millivolts or lower to about 600 millivolts is applied to network 131, and when at the lowest level, draws a highest level of current flow through network 131, which current flow applied to ground 126 reduces potential on emitter 119 to a level to bias transistor

123 to a higher impedance, reducing output on collector 134 to 0 volts. As the signal applied to network 131 increases, less current flows through resistor 128, increasing a potential at terminal 140 and biasing transistor 123 to a more conductive state in direct relationship with the input signal, shifting current flow to the load via transistor 123 and increasing voltage drop thereacross. In the event the input signal exceeds the reference potential applied to terminal 152, as by a noise spike, biasing transistor 123 into saturation, the load is generally protected from an over-voltage condition due to the constant current source 136 providing only 9.33 milliamps current flow to the load.

Referring now to Fig. la, there is shown a largely schematic electrical diagram of the invention. A computer 10 provides three, blue (SB), red (SR), and green (SG), analog color signals and vertical (SV) and horizontal (SH) synchronization signals.

As shown, the three color signals are supplied to three like transmitter circuits 12, 14, and 16, one of which, circuit 12, is shown in detail. The synchronization signals SV and SH are supplied to time multiplexer 18 which conventionally time multiplexes these signals and provides a combined output signal S to an input of cross-switcher 34.

Referring first to transmitter circuit 12, the input signal SB, the blue video signal, is supplied by computer 10 to transmitter 12. Signal SB and the other color outputs of computer 10 each typically vary over a range from 0 to 750 my, and need frequency response up to about 200 MHZ.

Referring to Fig. la, transistor Q9 receives on its base an SB signal, across resistor 36 from computer 10, and basically serves as a buffer, providing, from its emitter, an input through resistor R35 to the base of transistor Q10 of differential amplifier 26. The emitter of transistor Q9 is D.C. biased through resistors R35 and R38 from a five-volt + terminal, designated V_{CC} throughout Fig. 1. The base of transistor Q10 is biased through resistor R38, and capacitor C7 provides a decoupling effect across the V_{CC} terminal. The collector of transistor Q9 is connected to ground.

Transistors Q10 and Q12 are coupled, as will be described, as a differential amplifier 26 providing high frequency boost. The emitter of transistor Q10 is biased through resistors R40 and R51 from the V_{CC} and the V_{CC} is decoupled at resister R51 by capacitor C19. The emitters of transistors Q10 and Q12 are connected by resistor R40 and by a series of RC high frequency boost filter circuits, as will be discussed below. The emitter of transistor Q12 is D.C. biased from the V_{CC} through resistor R51.

The base of transistor Q12 is biased through resistor R39 from the V_{CC} as effected by the load manifested at junction SJ1. A portion of this load is manifested from D.C. restorer 45 as driven by differential amplifier 26, shown in greater detail in Fig. 2. The net effect of this is a closed loop feedback that receives the voltage appearing at the base input of transistor Q12 which, of course, varies. This in turn varies the total current feeding the amplifier through resistor R51, and the balance of current is split

between transistors Q10 and Q12 to maintain truly balanced outputs.

It is to be noted that this balanced output of differential amplifier 26 appears across the combination of transistor Q10 collector resistor R37 and transistor Q12 collector resistor R43.

As suggested above, and significantly, differential amplifier 26 provides several stages of high frequency boost as shown by RC circuits RCl-RC6 and C29, connected between the emitters of transistors Q10 and Q12.

The emitters of transistors Q10 and Q12 are also coupled by resistor R40, which is of a value of approximately 118 ohms and acts as the D.C. gain of the circuit.

High frequency boost stages RCl, RC2, and RC3, each consisting of a resistor and a capacitor in series, and each have a discrete time constant accomplished by sizing, of the capacitor of the stage to achieve a high frequency boost for different portions of the spectrum of interest from 0 to 200 MHZ.

In addition, there are provided three selectable high frequency boost stages, RC4, RC5, and RC6, each of which is switched in or out by a switch 56 shown in the open position. In operation, one or more of these switches would be closed as 'deemed necessary as a direct function of the length of cable to be used and as a function of the condition of the twisted pairs employed. Thus, RC4, RC5-, and RC6 would additively be

inserted as it appeared necessary to achieve the desired degree of signal purity at monitor 69 (Fig. 1b).

As shown in Fig. 2, a sample of the output of differential amplifier 26, taken across collector-resistors R37 and R43, is fed to operational amplifier U2 through resistors R41 and R44. A negative feedback path is provided by capacitor C31 from the output of operational amplifier U2 to its inverting input.

The output of operational amplifier t32 is fed to the base input of transistor Q11, there being capacitor C28 connected between the base of it and ground, which capacitor is sized, e.g., 22 μF to 100 μF to stabilize the base voltage of transistor Q11. The emitter of transistor Q11 is connected to the base of transistor Q12 at summing junction SJ1, and the collector of transistor Q11 is grounded. As one function of transistor Q11, transistor Q12 receives a base voltage raised by a diode drop through transistor Q11, a like raise as provided by transistor Q9 to transistor Q10 (Fig. la), to basically balance the DC. levels of the two. In this respect, transistor Q11 functions as a part of D.C. restorer 45 and functions for the purpose of stabilization as well as providing an offset voltage to the base of transistor Q12 of differential amplifier 26 to match that provided by transistor Q9.

Referring back to Fig. la, the output of transmitter circuit 12 appears across collector-resistors R37 and R38, each connected to ground, and together providing a balanced output. These resistors each have a value of approximately 50 ohms to, together, match

the rather standard impedance of 100 ohms of twisted pair telephone lines, such as T1-T4 of cable 57.

Each of transmitter circuits 14 and 16 are identical with that of transmitter circuit 12, and thus together they apply blue (B), red (R), and green (G) input signals to discrete input ports P_1-P_3 of cross-switcher 24.

Multiplexer 18 time multiplexes the vertical and horizontal signals SV and SH from computer 10, and the resulting signal is applied as an input S to a discrete port P_4 of cross-switcher 34. It has an output impedance of 100 ohms to match a twisted pair T4 of cable 57. Thus, in all, there are four signal inputs to cross-switcher 34.

Basically, cross-switcher 34 is configured to connect any one of its input signals at ports P_1-P_4 to any one of its output ports $P0_1$-$P0_4$, to which any particular pair of twisted pairs T1-T4 of a cable, having various arrangements of twisted pairs and twist rates, may be connected. Thus, as shown, cable 57, a common cable, has four twisted pair conductors, T1-T4, and these are connected to discrete output ports $P0_1$-$P0_4$ of cross-switcher 34. This enables the systematic employment of cable manufactured by a number of different manufacturers, with a variety of twist rates for individual twisted pairs to be selectively coupled, as will be described. Typically, all twisted pairs of a cable have twist rates which differ as between pairs, to prevent cross-talk in normal telephone usage.

Here, the magnitude of twist rate is used to designate cable pairs, this being from an examination wherein it has been found that cable pair T1 has the lowest twist rate, and cable pair T4 has the highest or largest twist rate. Applicants have determined that the connection pattern of cross-switcher 34 would be such that the S output of multiplexer 18 would be connected to a cable pair T4 of cable 57, it having the highest twist rate and thus the longest length. This follows from the determination that its twist rate and thus its inherent longest signal delay is not usually critical.

The B or blue output from transmitter circuit 12 would be connected to the twisted pair T3 having the next lower twist rate; the G or green output from transmitter circuit 16 would be connected to the next lower twist rate pair, T2. The R or red output of transmitter circuit 14 would be connected to the lowest rate cable pair T1 of cable 57 thus having the shortest overall length.

The relative twist rates of twisted pairs can be determined by a visual inspection of approximately six inches of the cable being examined, and therefrom connections would be arranged in terms of the foregoing system of connection.

The length of cable 57 would typically be in the approximate range of from 300 up to about 1,500 feet.

Referring to Fig. 1b, twisted pairs T1-T4 terminate in the order of input ports P_1-P_4 of connector 67. Connector 67 effects a connection between input ports P_1-P_4 of these cable pairs to a

series of its coordinate outputs $P0_1$-$P0_4$, including those labeled simply R (red) , G (green) , B (blue) , and S (synchronization) in this same order.

As a feature of this invention, for cables of a length of shorter than about 300 feet, the outputs would be directly connected to the same designated color inputs or receivers 74, 76, and 78 through cross-switcher 73, performing a like function to that of cross-switcher 34 as shown in parenthetically enclosed small letters. Also, as shown in Fig. 1b, this is effected by the closure of switches 51 and 52 to bypass time delay units 61 and 63. This configuration arises from the discovery that with shorter length cables (<300 feet), cable pairs may be employed with different twist rates where they carry the particular colors as shown and still provide adequate signal purity without time compensation.

Demultiplexer 66 is fed an S signal from $P0_4$ of connector 67, and this signal is then. separated back into horizontal H and vertical V signals and to thus be directly applied to analog monitor 69.

For greater lengths, and as a further feature of this invention, the green and red signals are delayed. Thus, with this mode of operation, cross-switcher 73 is adjusted such that input P_1, the red input, is connected to either the $P0_2$ or $P0_3$ output, and the green input at P_2 is connected to the other of the $P0_2$ or $P0_3$ output. Input P_3 of cross-switcher 73, the blue input, is connected to output $P0_1$. The position of particular color outputs of the

cross-switcher are shown in capital letters B, G, and R. Delays units 61 and 63 are in circuit with the red and green signals, and the delay units are adjusted to compensate for the particular added lengths of twisted pairs T2 and T3 when compared with the length of twisted pair T1. Thereby, the time of arrival of the signals at monitor 69 can be adjusted so that all three signals arrive at the same time. There is, as shown, additional signal processing by receivers 74, 76, and 78, as will be further discussed below.

Figs. 3-5 illustrate the construction of one of the delay units of delay units 61 and 63 of Fig. 1b as delay unit 64. Thus, a delay unit 64 is formed with a dielectric base or insulating board 70 such as fiberglass, typically used in printed circuit boards. A printed conductor 62 is on one side, and directly opposite on the other side is printed conductor 65. Thus, with such parallel conductors separated by an insulating board 70, there is created discrete lengths of balanced transmission lines, as illustrated in Fig. 5. The thickness and material of the board determine a dielectric coefficient which basically determines the characteristic impedance of the transmission line, which in this case has been chosen with a thickness of 0.032 inch to create a transmission line having about the same propagation factor as twisted pair lines T1-T4 and with a like characteristic impedance of approximately 100 ohms, matching the usual or standard impedance of the twisted pair communications lines. The propagation factors of both the twisted pair lines and transmission line are approximately 0.69.

As shown in Fig. 5, each of the separate transmission lines D1-D5 of conductor pairs 62 and 65 are of the same length and are compressed by the serpentine arrangement to fit an approximately 4½x7 inch board 70. The conductors have a width of approximately 0.028 inch and thickness of approximately 0.0015 inch and are typically constructed of printed circuit board copper trace. The conductors have break points as illustrated in Fig. 5 wherein, in practice, the lengths of the separate delay lines, Dl, D2, D3, D4, and D5, each have an actual length of approximately 65 cm to create a delay of 5 nanoseconds or a total delay of 25 nanoseconds.

Referring further to Fig. 5, an input signal to signal pair 80 of delay unit 64, as from cross-switcher 73 (Fig. 1b), connects to terminals 82 and 84, one of them, terminal 82, being attached to a conductor of pair 80 on the reverse side of board 64, and terminal 84 being connected to the other conductor of pair 80 on the top side of board 70. Similarly, a signal output line 83, to one of receivers 74 or 76, would have its conductors connected to conductor terminal 81 on the top side of board 64, and terminal 85 on the bottom side of board 70.

Circuit connections are variably made for different delays by means of straps, for example, a strap 96, on each side of board 70 would connect in circuit any number of delay units Dl, D2, D3, D4, and D5. Again, only the unit conductor terminals for the one side are shown, it being understood that the same designation and pattern of terminals and straps is provided on the opposite side,

and the same pattern of strapping between units would be accomplished.

Thus, in order to employ a minimum delay, utilizing delay line Dl, terminals 92 and 94 would be strapped together by a strap 96, whereby, as is apparent, only delay unit Dl would be in circuit between input and output signal lines 80 and 83 for a delay of 5 nanoseconds.

If it is desired to add another 5 nanoseconds of delay, straps 96 would interconnect terminals 92 and 102, and strap 106 would interconnect terminals 104 and 105. Following the same pattern of connection, if additional delay is needed, a strap would interconnect one of terminals 109, 111, 113, or 115, with an opposite terminal of terminals 110, 112, 114, or 116, and preceding straps would be employed in the fashion illustrated to further serialize delay units D3, D4, and/or D5.

As described, and referring to Fig. 1b, two of the delay units 64, as delay units 61 and 63 (Fig. 1b), would typically be employed, one in circuit with each of twisted pairs from terminals $P0_2$ and $\overline{P0_3}$ of cross-switcher 73, being the conductor pairs having the smaller of the twist rates of the three conductor pairs (for color signals), being for the green and red color signals. Thus, in the illustration, the applicants have chosen to connect via cross-switcher 73, at the far end of cable 57, the red signal R and green signal G to twisted pairs T2 and T3. The green and red signals are connected to signal delay units 61 and 63, respectively, and the blue or B signal connected directly to the P_1 input of cross-

switcher 73. The switched delays set forth for each board 64 would be such as to compensate for the differences in lengths of twisted pairs and produce an essentially equal path for each color transmission. This may be accomplished by observing monitor 69. Alternately, the transmission lines, with appropriate input and output couplers (providing an input and output to an unbalanced line), may be unbalanced lines where in there would simply be a conductive plate on one side of board 70 and only the conductors on the opposite side are employed and are switchable.

The discrete outputs of cross-switcher 73 are connected, as shown, to the discrete balanced inputs of identical receivers 74, 76, and 78, receiver 74 being shown in detail. Examining receiver 74 (Fig. 1b), a receiver input from terminal output PO_1 obtains a signal appearing across resistors R15 and R23 balanced to ground through capacitor C203. The input across R15 is applied through capacitor C17 to the base input of transistor Q1, and the other input is applied across resistor R23 and through capacitor C23 to the base input of transistor Q2. These two transistors are connected and operate as a differential amplifier 110.

Referring now additionally to Fig. 6, the bases of transistors Q2 and Q1 are biased through separate paths, one being through R25, R24, and R22 to the base of transistor Q2 and through resistors R25, R24, and R14 to the base of transistor Q1. Bias is from a positive source terminal V_{CC}, and it is bypassed to ground through capacitor C11. The base bias to transistors Q2 and Q1 as it appears at summing junction SJ2 is also effected by the emitter

voltage of transistor Q4 of buffer 120. Buffer 120 is in turn driven by the collector output of transistor Q2 taken across collector-resistor R36 and a high frequency attenuator 122, which functions to roll off excess energy on the video signal (i.e., overshoot) to enhance signal purity to monitor 69. The control of transistor Q4 is described below with respect to a further description of Fig. 6.

The emitters of transistors Q2 and Q1 are supplied current and bias control by control 130 (Fig. 1b) which employ transistor Q5 (Fig. 6) by receiving a voltage bias on its base. The emitter bias to transistors Q1 and Q2 is supplied from the collector of transistor Q5 through resistors R13 and R21, respectively, and the amplification of this current is set by the magnitude of resistor R26 and the emitter voltage of transistor Q5.

Differential amplifier 110, which is basically formed by transistors Q2 and Q1, includes a high frequency boost circuit and wherein there are four serially-connected RC circuits RC7, RC8, RC9, and RC10, each circuit connected between the emitter of transistors Q2 and Q1 and each having a time constant to deal with discrete portions of the desired frequency response boost, from D.C. to 200 MHZ. Additionally, capacitor C8, also connected between the emitters of transistors Q2 and Q1, has a value of approximately 150 pF and functions to add selected high frequency boost as necessary and as a direct function of the length of transmission line.

As in this case, it is desired to obtain only a single-ended output of differential amplifier 110, a single load resistor, being

R36, is connected between the collector of transistor Q2 and ground, and the collector of transistor Q1 is directly grounded. The output of differential amplifier 110, across resistor R36, is buffered through transistor Q7 (Fig. 6), and its emitter provides the blue signal to monitor 69.

As noted above, Fig. 6 separately illustrates circuitry for providing an additional biasing effect to the bases and emitters of transistors Q1 and Q2, this being present at summing junction SJ2 and effecting the emitter biasing by control of emitter bias control 130 (Fig. 1b).

Referring again more particularly to Fig. 6, a sample signal input for the circuitry is obtained across receiver output resistor R36 and high frequency attenuator 122, as discussed above, and is applied to the base input of transistor Q7 of a buffer stage including transistors Q7 and Q10 wherein the collector output of transistor Q7 is fed to the base input-of transistor Q10 and the two providing, as described above, a buffer which drives monitor 69.

To effect operation, a D.C. bias is applied from a V_{CC} A.C. bypassed by capacitor C21, through resistor R35 to the emitter of transistor Q10a and additionally through resistor R34 to the base of transistor Q10a and collector of transistor Q7. The output of this amplifier or buffer stage at the connected emitter of transistor Q7 and collector of transistor Q10 is fed directly to monitor 69 and through resistor R33 to the base of transistor Q9a of differential amplifier stage 71 of D.C. restoration circuit 124.

Differential amplifier 71 basically employs transistors Q9a and Q8, and the emitters are connected together and biased by a +, or V_{CC} terminal through resistor R16. The base of transistor Q9a is biased through resistor R32 from a V_{CC} terminal, and the base of transistor Q8 is biased through resistor R28 from the V_{CC}. Resistor R27, bypassed by stabilizing capacitor C23, is connected between the base of transistor Q8 and ground. The collector output of transistor Q6, appearing across capacitors C21 and C19 as stabilizing capacitors, is connected to the base input of transistor Q4. The collector of transistor Q4 is connected to ground, and a stabilizing capacitor C20 is connected between the emitter and ground, with the result that a restored D.C. voltage is applied to summing junction SJ1, at which point the conventional bias from the V_{CC} and the effect of emitter-collector reaction of transistor Q4 meet, with the result that this voltage plus base currents from transistors Q1 and Q2 across resistors P14 and R22 provide D.C. bias for D.C. restoration circuit 124.

Thus, as one effect of the above, the voltage drop across resistor 25, bypassed to ground by capacitor C15 and applied to the base bias of transistor Q5, determines the amount of current supplied to differential amplifier 110 through resistors R13 and R21. Finally, a V_{CC} terminal is connected through resistor P26 to the emitter of transistor Q5, and the collector of this transistor provides a current limitation characterized type bias through resistors R13 and R21, respectively, to emitters of transistors Q1 and Q2.

As a result of the base bias voltages, derived as stated, to transistors Q1 and Q2 and the emitter biases to transistors Q1 and Q2 as just described, there is effectively created a feedback system which modulates supply current to transistors Q1 and Q2 at a voltage to maintain the collector outputs of transistors Q1 and Q2 within a selected range, as at the output of transistor Q2 and across resistor R36. Accordingly, there is provided an-optimum single-ended video signal for the base of transistor Q7 and an optimum output to monitor 69.

Receiver 74 thus functions to provide a high frequency boost by virtue of the RC circuits 7, 8, 9, 10, and C8 which effects A.C. gain and phase shifts at various frequencies in the frequency region up to 200 MHZ and thus to achieve a final frequency compensated signal response to monitor 69.

Referring back to Fig. 1b, the output of receiver 74, as thus boosted by the RC circuits illustrated and as attenuated by attenuator HFA 122, is buffered and then fed as a blue input to analog color monitor 69, as described.

Green and red receivers 76 and 78 are illustrated only in block form and function as receiver 74, as described above. The outputs of the receivers are provided to monitor 69, being a green signal as the output of receiver 76 and as a red signal of the output of receiver 78. With the frequency compensation and delay adjustments described above, there is provided to monitor 69 a coordinate signal wherein the interconnections and timings of the color signals are such as to provide a composite signal with

excellent color quality despite the most unlikely medium of cable transmission. Again, the adjustments are simply to adjust the filter insertions and delay insertions, as described above, to effect optimum quality.

Most significantly, this invention provides a means of color communications in literally thousands of locations having twisted pair installations at low cost which otherwise could cost the users quite large sums as required to replace twisted pair telephone lines with conventional high frequency conductors.

While the invention has been particularly shown and described with reference to embodiments thereof, those skilled in the art will understand that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the present invention.

WHAT IS CLAIMED IS:

1. A system for transmitting analog color video signals having color video components, comprising:

an interface to a cable having multiple twisted pairs, said pairs having varying twist rates relative to each other, said interface selectively coupling said pairs to carry selected ones of said color video components as a function of the varying relative twist rates.

2. A system according to claim 1, wherein the interface includes:

at least one transmitter to boost a signal strength of at least one of said color video signal components.

3. A system according to claim 2, wherein the interface further comprises:

at least two transmitters to boost signal strengths of corresponding ones of said color video signal components, said transmitters characterized by respectively differing gains.

4. A system according to claim 1, wherein the interface further comprises:

a cross switch to receive the color video signal components and apply the color video signal components to corresponding ones of the twisted pairs.

5. A system according to claim 1, wherein the cross switch further receives a sync signal of said analog color video signal and applies said sync signal to another of said twisted pairs.

6. A system according to claim 1, further including:

a computer to provide the analog color video signals having color video signal components.

7. A system according to claim 1, wherein the color video components include a red component and said interface selectively couples one of said twisted pairs having a lowest relative twist rate to the red component.

8. A system according to claim 1, wherein the color video components include a green component and said interface selectively couples one of said twisted pairs having a non-minimum relative twist rate to the green component.

9. A system according to claim 1, wherein the color video components include a blue component and said interface selectively couples one of said twisted pairs having a non-minimum relative twist rate to the blue component.

10. A system according to claim 1, wherein the color video components include a red, green, and blue component and said interface selectively couples a first of said twisted pairs having a lowest relative twist rate to the red component, a second of said twisted pairs having a next-lowest relative twist rate to the green

component, and a third of said twisted pairs having a third-lowest relative twist rate to the blue component.

11. A system according to claim 1, wherein:

the color video components include a red, green, and blue component and a sync signal;

the cable includes four twisted pairs having respectively a first lowest relative twist rate, a second lowest relative twist rate, a third lowest relative twist rate, and a highest relative twist rate; and

said interface selectively couples the red component to said twisted pair having the first lowest relative twist rate, the green component to said twisted pair having the second lowest relative twist rate, the blue component to said twisted pair having the third lowest relative twist rate, and the sync signal to said twisted pair having the highest relative twist rate.

12. A system for receiving analog color video signals having color video components, comprising:

an interface to a cable having multiple twisted pairs, said pairs having varying twist rates relative to each other and carrying selected ones of said color video signal components, said interface imposing different relative signal delays on said color video components as a function of the varying relative twist rates.

13. A system according to claim 12, wherein the interface further includes:

a connector coupled to the twisted pairs, and

a cross switch coupled to the connector to selectively re-impose said signal delays to different ones of said color video components.

14. A video signal communicator, comprising:

an input to receive a plurality of analog components of a video signal;

a cable having a plurality of twisted pairs, at least two of said pairs having different relative twist rates;

a transmission interface, coupled to the cable, to receive the plurality of analog components and apply said plurality of analog components to said plurality of twisted pairs such that a selected first one of said analog components travels on a first one of said twisted pairs having a first relative twist rate and a selected second one of said analog components travels on a second one of said twisted pairs have a second relative twist rate different from the first relative twist rate;

a reception interface, coupled to the cable, to receive the plurality of analog components from said plurality of twisted pairs.

15. A video signal communicator according to claim 14, wherein:

the input is a connector port to receive the plurality of analog components of the video signal from a computer.

16. A video signal communicator according to claim 14, further including:

an output connector port coupled to the reception interface to apply the plurality of analog components of the video signal to a monitor.

17. A video signal communicator according to claim 14, wherein:

the cable includes four twisted pairs having variable relative twist rates, and the plurality of analog components of the video signal include three analog components applied by the transmission interface to three of the four twisted pairs.

18. A video signal communicator according to claim 14, wherein:

the plurality of analog components of the video signal include three analog components; and

the transmission interface includes a switch to selectively apply the three analog components to selected ones of the plurality of twisted pairs.

19. A video signal communicator according to claim 14, wherein:

the three analog components include a red component, a green component, and a blue component, and

the transmission interface applies the red component to one of said twisted pairs having a first lowest relative twist rate, the green component to one of said twisted pairs having a second lowest relative twist rate, and the blue component to one of said twisted pairs having a third lowest relative twist rate.

20. A video signal communicator according to claim 14, wherein:

the three analog components include a red component, a green component, and a blue component, and

the transmission interface includes a switch to selectively apply the three analog components to selected ones of the plurality of twisted pairs, wherein the switch defaults to apply the red component to one of said twisted pairs having a first lowest relative twist rate, the green component to one of said twisted pairs having a second lowest relative twist rate, and the blue component to one of said twisted pairs having a third lowest relative twist rate.

21. A video signal communicator according to claim 19, wherein:

the analog color video signals also include a sync signal; and

the transmission interface also applies the sync signal to one of said twisted pairs having a highest relative twist rate.

22. A video signal communicator according to claim 14, wherein the reception interface includes at least one delay circuit corresponding to at least one of said twisted pairs to impose a signal delay on said analog component received from said at least one twisted pair.

23. A video signal communicator according to claim 14, wherein the reception interface includes two delay circuits corresponding to two different ones of said twisted pairs to impose different signal delays on said analog components received from said different ones of said twisted pairs.

24. A video signal communicator according to claim 23, wherein:

the reception interface includes a switch to selectively apply the three analog components to selected ones of the two delay circuits.

25. A method of transmitting color video signals over a cable having a plurality of twisted pairs having varying twist rates, comprising the steps of:

ranking the twisted pairs according to their twist rates;

applying selected components of the color video signals to the twisted pairs in accordance with the ranking.

26. A method according to claim 25, wherein the step of applying includes the step of:

applying a red component of the color video signal to a twisted pair having a lower relative twist rate.

27. A method according to claim 25, wherein the step of applying includes the step of:

applying a green component of the color video signal to a twisted pair having a non-minimum relative twist rate.

28. A method according to claim 25, wherein the step of applying includes the step of:

applying a blue component of the color video signal to a twisted pair having a non-minimum relative twist rate.

29. A method according to claim 25, wherein the step of applying includes the step of:

applying a synchronization signal of the color video signal to a twisted pair having a highest relative twist rate.

30. A method according to claim 25, wherein the step of applying includes the step of:

applying components of the color video signal to selected twisted pairs having the lowest relative twist rates.

31. A method according to claim 25, wherein the step of applying includes the step of:

applying a red component of the color video signal to a twisted pair having a lower relative twist rate;

applying a green component of the color video signal to a twisted pair having a moderate relative twist rate;

applying a blue component of the color video signal to a twisted pair having a higher relative twist rate; and

applying a synchronization signal of the color video signal to a twisted pair having a highest relative twist rate.

32. A method of receiving color video signals over twisted pairs having non-uniform relative twist rates, comprising the steps of:

ranking the twisted pairs in accordance with their relative twist rates;

receiving components of the color video signals from different ones of the twisted pairs; and

delaying at least one component of the color video signals as a function of the ranking.

33. A video system for communicating video on twisted pair communication lines having variable inherent propagation delay rates, comprising:

video inputs providing respective components of a color video signal,

a first transmitter coupled to a first of said video inputs, comprising:

an input buffer coupled to receive a first of said respective components of the color video signal, and

a differential amplifier coupled to the input buffer and providing a high frequency boost to the first of said respective components, and

an output coupled between the differential amplifier and a first of said communication lines to communicate video component information identifying the first of said respective components to the first of said communication lines, and

a first switch coupled to the twisted pair communication lines to apply said video component information to a selected one of said twisted pair communication lines.

34. A video system according to claim 33, further comprising:

a second switch communicating with a distal end of said twisted pair communication lines to receive said video component information from said selected one of said twisted pair communication lines,

a delay circuit communicating with said second switch to receive said video component information, and

a monitor output coupled to deliver said video component information to an external video monitor.

35. A video system according to claim 33, wherein

said video inputs provide respective red, green and blue components of an analog color video signal.

36. A video system according to claim 33, wherein

the input buffer is a transistor having a base connected to receive the first of said respective components of the color video signal and an output connected to deliver the first of said respective components to the differential amplifier.

37. A video system according to claim 33, wherein

the differential amplifier further includes a filter to tune said high frequency boost to the first of said respective components.

38. A video system according to claim 37, wherein

the differential amplifier includes first and second transistor amplifiers, a gate of said first transistor amplifier coupled to receive the first of said respective components from said input buffer, and inputs to said first and second transistor amplifiers being coupled to said filter.

39. A video system according to claim 38, wherein

said first and second transistor amplifiers include respective outputs coupled to deliver said video component information, and

a gate of said second transistor amplifier is coupled to said output of said second transistor in a closed feedback loop.

40. A video system according to claim 39, wherein the closed feedback loop includes a D.C. restorer circuit.

41. A video system according to claim 34, wherein

said delay circuit also includes a switchable bypass circuit to selectively bypass said delay circuit.

42. A video system according to claim 34, further including

a receiver communicating with the delay circuit, said receiver including:

a differential amplifier circuit to boost a high frequency response of said video component information.

43. A video system according to claim 42, wherein the differential amplifier further includes a filter circuit to tune said high frequency response.

44. A video system for communicating video on twisted pair communication lines having variable inherent propagation delay rates, comprising:

a transmitter, comprising:

video inputs providing red, green and blue components of a color video signal,

first, second and third transmitter processing circuits coupled to, respectively, first, second and third ones of said video inputs, each of said transmitter processing circuits including:

a differential amplifier tuned to boost predetermined frequency portions of said red, green and blue components,

first, second and third output pairs coupled between the respective differential amplifier and first, second and third ones of said twisted pair communication lines to communicate video information signals identifying said red, green and blue components from said respective differential amplifiers, and

a first switch coupled to a proximal end of said twisted pair communication lines to apply corresponding ones of said video information signals identifying said red, green, and blue

components to selected ones of said twisted pair communication lines based on said variable inherent propagation delay rates, and

a receiver comprising:

a second switch communicating with a distal end of said twisted pair communication lines to receive the video information signals identifying said red, green and blue components from said selected ones of said twisted pair communication lines,

first, second and third input pairs coupled to the second switch to receive on selected ones of said input pairs the video information signals,

first, second and third receiver processing circuits coupled to, respectively, the first, second and third input pairs, each of said transmitter processing circuits including:

a differential amplifier tuned to boost predetermined frequency portions of said video information signals, and

a monitor port coupled to deliver said video component information to an external video monitor.

45. A video system according to claim 44, wherein the receiver further includes:

a green delay circuit between one of said differential amplifiers of said receiver and one of said input pairs corresponding to the green video component.

46. A video system according to claim 45, wherein the green delay circuit further includes a switchable bypass circuit to bypass the green delay circuit.

47. A video system according to claim 44, wherein the receiver further includes:

a red delay circuit between one of said differential amplifiers of said receiver and one of said input pairs corresponding to the red video component.

48. A video system according to claim 47, wherein the red delay circuit further includes a switchable bypass circuit to bypass the red delay circuit.

49. A video system according to claim 44, wherein the receiver further includes:

a green delay circuit having a first delay factor and being between one of said differential amplifiers of said receiver and one of said input pairs corresponding to the green video component, and

a red delay circuit having a second delay factor different from the first delay factor and being between another of said differential amplifiers of said receiver and another of said input pairs corresponding to the red video component.

50. A video system according to claim 49, wherein the red and green delay circuits further each include a switchable bypass circuit to respectively bypass the red and green delay circuits.

51. A video system according to claim 49, wherein said input pair corresponding to the blue video component has substantially no corresponding blue delay circuit.

52. A transmission system for coupling video color signals including red, green, and blue video components to corresponding twisted pair communication lines, including:

a circuit to impose a discrete signal delay on at least one of the video components as a function of a discrete first rate in a corresponding one of said twisted pair communication lines.

ABSTRACT OF THE DISCLOSURE

A transmission system for transmitting analog color video signals wherein a cable comprising multiple twisted pairs is employed, and certain of these pairs are coupled to carry selected color signals as a function of the delay provided by particular twist rates. In certain instances, selected signal delay devices are connected in circuit with certain twisted pairs. By such an arrangement, it has been found that relatively long distances between a computer and a monitor may be spanned by relatively low-cost, twisted pair cable commonly used for telephone communications.

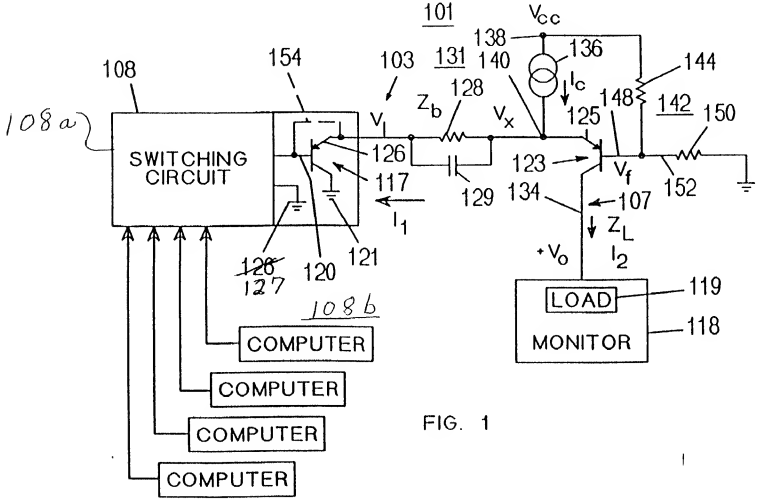
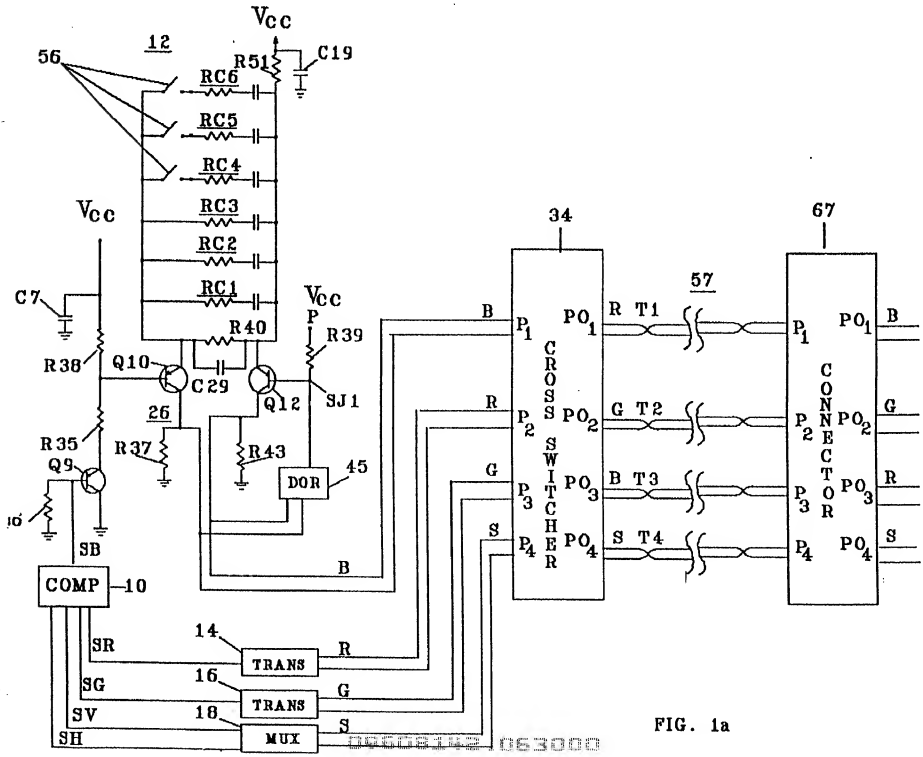


FIG. 1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12
56
R51
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RC5
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RC3
RC2
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Vcc
C7
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Q10
C29
Q12
SJ1
26
R35
R37
R43
DOR
45
Q9
SB
COMP
10
B
R
G
S
14
TRANS
SR
16
TRANS
SG
18
MUX
SV
SH
34
CROSS SWITCHER
P1
P2
P3
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PO2
PO3
PO4
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G T2
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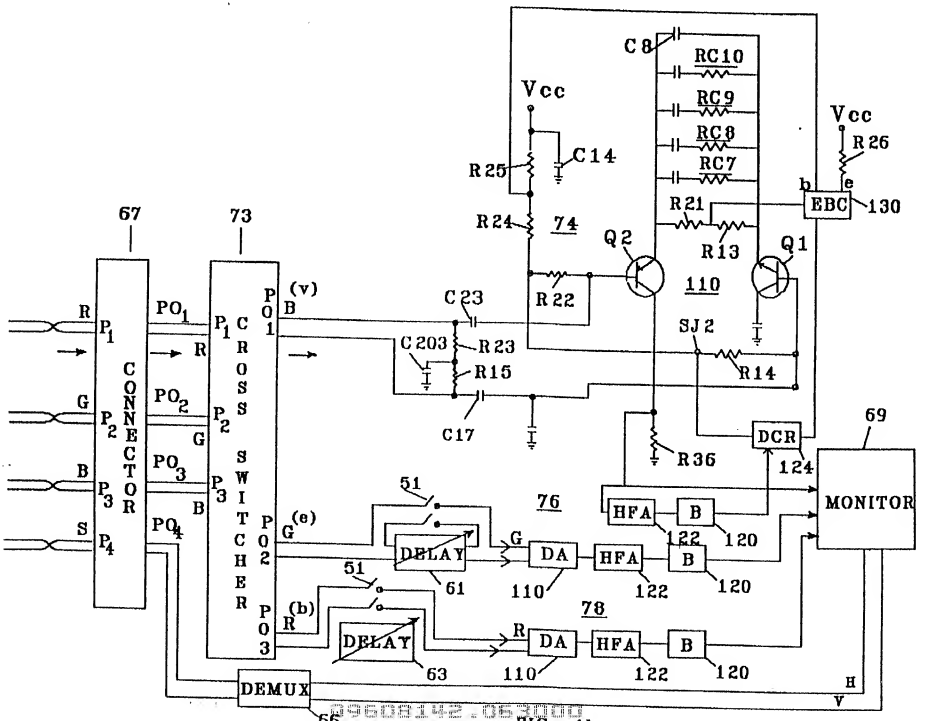
S T4
57
67
CONNECTOR

FIG. 1a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S
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P2
P3
P4
PO1
PO2
PO3
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(e)
(b)
C8
RC10
RC9
RC8
RC7
Vcc
C14
R25
R24
74
R21
R13
Q2
Q1
R22
110
C23
C203
R23
R15
C17
SJ2
R14
R36
R26
b
e
EBC
130
DCR
124
69
MONITOR
51
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DELAY
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DA
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HFA
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DEMUX
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H
V

FIG. 1b

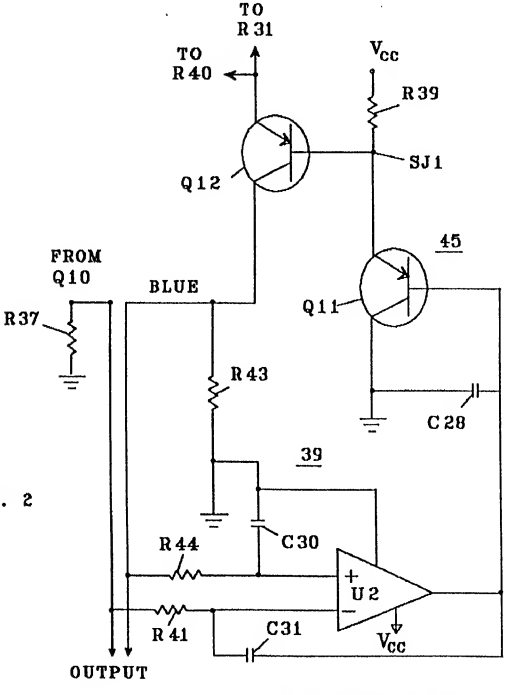


FIG. 2

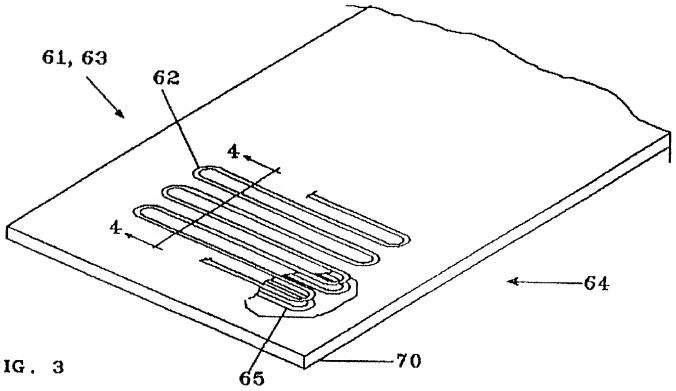


FIG. 3

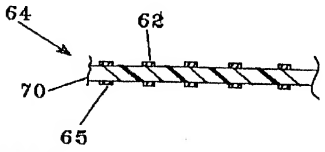
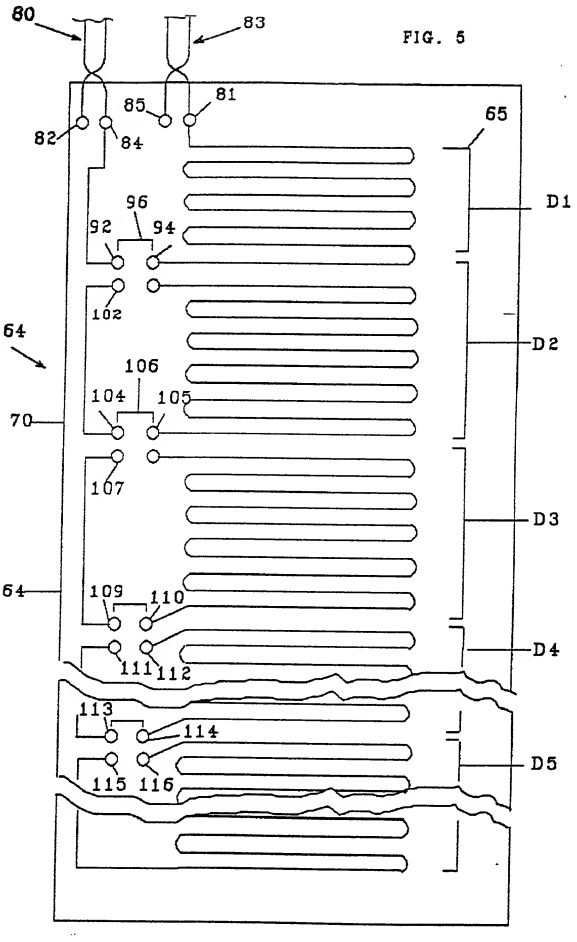


FIG. 4

FIG. 5


80
83
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84
65
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D1
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D2
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D3
64
109
110
D4
111
112
113
114
D5
115
116

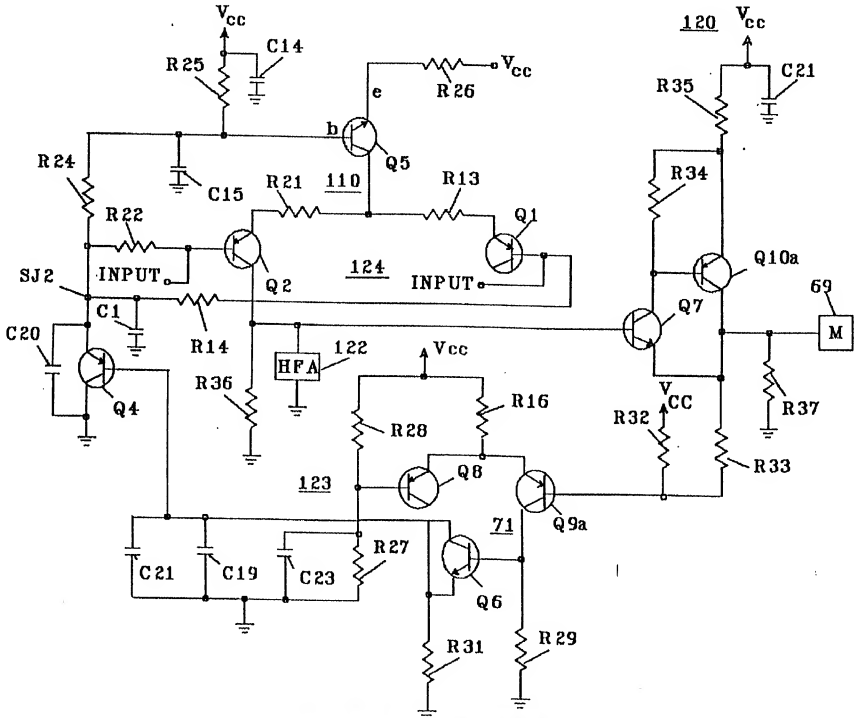
Vcc
C14
R25
e
R26
Vcc
b
Q5
R24
C15
R21
110
R13
R22
Q1
Q2
124
INPUT
INPUT
SJ2
C1
R14
C20
Q4
HFA
122
Vcc
R36
R16
R28
123
Q8
Q9a
71
C21
C19
C23
R27
Q6
R31
R29
120
Vcc
C21
R35
R34
Q10a
69
Q7
M
R37
VCC
R32
R33

FIG. 6

Nixon & Vanderhye P.C. (10/99)
(Domestic Assigned)

RULE 63 (37 C.F.R. 1.63)
INVENTORS DECLARATION FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"Twisted Pair Communications Line System"

the specification of which **(check** applicable **box(s))**:

☒ is attached hereto
☐ was filed on _____ as U.S. Application Serial No. _____ (Atty Dkt. No. 2540-248)
☐ was filed as PCT International application No. _____ on _____
And (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Priority Foreign Application(s):

Application Number	**Country**	**Day/Month/Year Filed**

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

Application Number	**Date/Month/Year Filed**

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT International applications listed above or below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): **Application Serial No.**	**Day/Month/Year Filed**	**Status: patented pending, abandoned**
09/294,591	20 April 1999	Pending
08/774,629	6 November 1996	Patented
08/660,076	3 June 1996	Pending
08/177,442	5 January 1994	Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon. And on behalf of the owner(s) hereof, I hereby ask that all communications in this matter be directed to:
NIXON & VANDERHYE P.C., 1100 North Glebe Rd., 8th Floor, Arlington, VA 22201-4714, telephone number (703) 816-4000.

3. Inventor's Signature: Steven F. Brown Date: 6/14/00
Inventor: **Steven** (first) **F.** MI **BROWN** (last) **USA** (citizenship)
Residence: (city) Huntsville (state/country) Alabama
Post Office Address: 300 Bay Hill Way, Huntsville, Alabama
(Zip Code) 35824

4. Inventor's Signature: Robert R. Asprey Date: 6/14/00
Inventor: **Robert** (first) **R.** MI **ASPREY** (last) **USA** (citizenship)
Residence: (city) Harvest (state/country) Alabama
Post Office Address: 104 Northwood Circle, Harvest, Alabama
(Zip Code) 35749

FOR ADDITIONAL INVENTORS, check box ☐ and attach sheet with same information and signature and date for each.

RULE 63 (37 C.F.R. 1.63)
INVENTORS DECLARATION FOR PATENT APPLICATION
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"Twisted Pair Communications Line System"

the specification of which (**check** applicable **box(s)**):

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☐ was filed on _____ as U.S. Application Serial No. _____ (Atty Dkt. No. 2540-248)
☐ was filed as PCT International application No. _____ on _____
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Priority Foreign Application(s):

Application Number	**Country**	**Day/Month/Year Filed**

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1. Inventor's Signature: Winston J. Stewart Date: 26 June 00
Inventor: **Winston** (first) **J.** MI **STEWART** (last) **USA** (citizenship)
Residence: (city) ~~Decatur~~ Hartselle (state/country) Alabama
Post Office Address: ~~369 E. Upper River Road, Decatur, Alabama~~ 1506 State St. NW
(Zip Code) ~~35603~~ 35604

2. Inventor's Signature: Date: 14 June 00
Inventor: **Philip** (first) **M.** MI **KIRSHTEIN** (last) **USA** (citizenship)
Residence: (city) New Market (state/country) Alabama
Post Office Address: 593 Sharpes Hollow Road, New Market, Alabama
(Zip Code) 35761

FOR ADDITIONAL INVENTORS, check box ☒ and attach sheet with same information and signature and date for each.